ACS APPLIED MATERIALS & INTERFACES

Letter

www.acsami.org

High-Performance Low-Voltage Organic Field-Effect Transistors Prepared on Electro-Polished Aluminum Wires

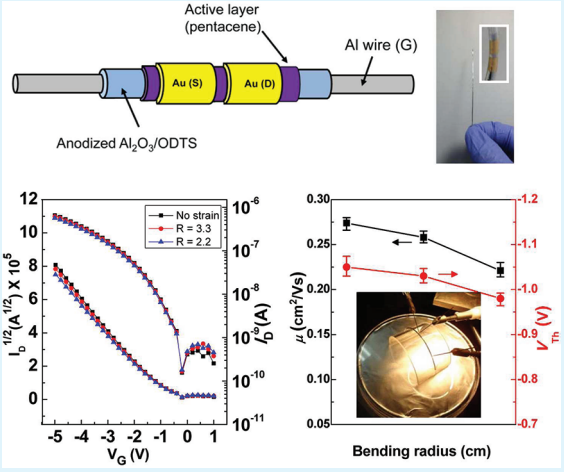
Sooji Nam,[†,‡,§] Jaeyoung Jang,[†,‡,§] Jong-Jin Park,[†] Sang Won Kim,[†] Chan Eon Park,*[,†,‡] and Jong Min Kim*[,†]

[†]Samsung Advanced Institute of Technology (SAIT), Yongin, 449-712, Republic of Korea

[‡]POSTECH Organic Electronics Laboratory, Polymer Research Institute, Department of Chemical Engineering, Pohang University of Science and Technology, Pohang, 790-784, Korea

Supporting Information

ABSTRACT: We report the preparation of high-performance low-voltage pentacene-based organic field-effect transistors (OFETs) fabricated on a metallic fiber (Al wire) substrate. The surface roughness of the wire was significantly reduced after 10 min of electro-polishing. A 120 nm thick Al_2O_3 gate dielectric layer was deposited on the anodized wire, followed by octadecyltrichlorosilane (ODTS) treatment. The ODTS-modified Al_2O_3 gate dielectrics formed around the Al wire showed a high capacitance of 50.1 nF cm^{-2} and hydrophobic surface characteristics. The resulting OFETs exhibited hysteresis-free operation with a high mobility of 0.345 cm^2 V^{-1} s^{-1} within a low operating voltage range of −5 V, and maintained their high performance at an applied tensile strain of bending radius ~2.2.



KEYWORDS: *low-voltage, bending-stability, hysteresis-free, metallic fiber, organic field-effect transistors, e-textiles*

Organic semiconductors have many advantages over their inorganic counterparts for use as active layers in low-cost flexible electronic devices, such as organic field-effect transistors (OFETs).[1−3] Because of their low processing temperature and mechanical flexibility, OFETs can be fabricated on plastic[1−3] or even on paper,[4] and are therefore considered to be essential for future electronics. OFETs show great potential in the field of e-textiles aimed at wearable electronics because their unique properties are compatible with cylindrical fiber-shaped substrates.[5−10] However, OFETs prepared on fiber-shaped substrates have not been extensively investigated and fully optimized, as the film deposition and device fabrication procedures are more difficult than for conventional planar devices.[10,11] In this case, solution-processing methods offer a simple low-cost route to forming uniform films with full coverage over a cylindrical substrate, in contrast with vacuum processing methods.[5,6,8,9]

Hamedi et al. demonstrated OFETs and electro-chemical transistors by creating junctions using an electrolyte lump as a gate dielectric at the intersection of two fibers (source/drain or gate fibers, respectively).[5,6] Although this approach is promising, a hygroscopic electrolyte with an extremely high permittivity should be used as the gate dielectric due to the very large thickness of the dielectric lump (>10 μm). These devices may be subject to drawbacks, such as hysteresis or gate-bias/mechanical bending stresses, unlike OFETs prepared using hydrophobic thin film gate dielectrics.[12−14] OFETs prepared on a cylindrical substrate with thin film gate dielectrics have been reported, using dip-coated polymer dielectrics[7−9] or vacuum-deposited oxide dielectrics.[10] However, these devices operate at very high voltages (>−20 V) due to the low capacitance of the gate dielectrics, which suggests that the devices should display a high power consumption.[7−10] Moreover, the electrical performance and bending stress-durability of these devices have been poor (mobility of <0.06 cm^2 V^{-1} s^{-1} and minimum bending radius of 8 cm), possibly due to the high surface roughness of the cylindrical substrates used (metallic fibers), in contrast with conventional planar silicon or glass substrates.[8] A rough surface can perturb formation of a smooth gate dielectric layer as well as formation of a highly crystalline organic semiconductor layer on the gate dielectric,[15] and can decrease the electrical strength of a gate dielectric by increasing the effective electric field.[16] High-performance devices with smooth dielectric surface have been achieved only for very thick polymer dielectric coatings

Received: August 23, 2011
Accepted: December 17, 2011
Published: December 17, 2011

(~ 1 μm) on fibers, but such thick polymer coating seriously increase the operating voltage.[8,9]

Therefore, the goals of (1) achieving smooth cylindrical substrates and (2) developing high capacitance gate dielectrics with hydrophobic surfaces using solution processes are needed to form well-ordered organic semiconductor thin films and to obtain low-voltage, hysteresis-free OFETs with high performance and bending stability. Here, we introduce a solution-processing approach that includes anodization followed by octadecyltrichlorosilane (ODTS) treatment to form a smooth hydrophobic gate dielectric layer on the cylindrical substrate. A metallic fiber (Al wire) was employed as a gate substrate, and the surface roughness of the substrate was significantly reduced by electro-polishing. Pentacene-based OFETs prepared on the Al wire substrate with a 120 nm-thick Al_2O_3/ODTS gate dielectric showed excellent electrical properties, stable operation against hysteresis/bending stresses, and a low operating voltage of −5 V. The performances of the devices on an Al wire are comparable to those of the conventional planar devices and even higher than those of the devices on an Al foil having the same device configuration.

Figure 1a shows a schematic diagram of the device structure for the OFETs prepared on an Al wire employed in this study.

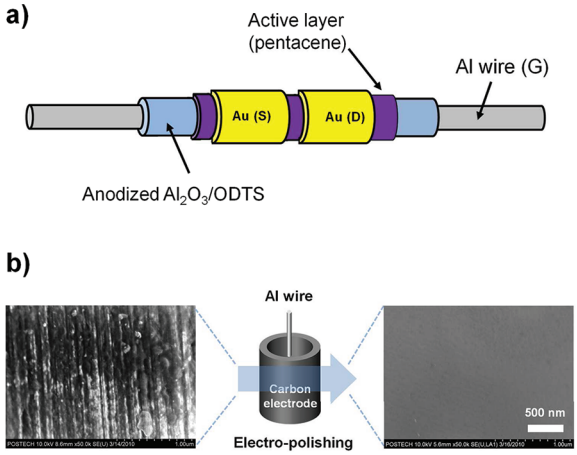


Figure 1. (a) Schematic diagram of the OFET device structures used in this study. (b) Schematic illustration of the electro-polishing process (center) and the SEM images of the Al wire surface before (left) and after (right) the 10 min electro-polishing process.

In general, manufactured metal wires (including Al wires used in this study) have extremely rough surfaces, as confirmed by the scanning electron microscopy (SEM) (S-4800, Hitachi) image on the left-hand side of Figure 1(b). To reduce the surface roughness, a wire (Aldrich) was electro-polished at a constant voltage of 20 V in a solution containing perchloric acid (60%):ethanol in a volume ratio of 1:4 at a constant temperature of 7 °C for 10 min using a cylinder-shaped carbon electrode, as shown in Figure 1b.[17] After polishing, the surface of the wire was much smoother, as shown in the left-hand SEM image of Figure 1b, and the radius (R) of the resulting wire was 350 μm, measured using calipers. The wire was then anodized with a constant current density of 0.32 mA cm^{-2} and a voltage of 80 V in a 0.05 M ammonium pentaborate octahydrate electrolyte solution at 25 °C using a cylinder-shaped carbon electrode to form a 120 nm thick Al_2O_3 layer around the Al wire gate substrate.[17−19] Subsequently, the anodized wire was dipped in a solution containing 60 μL o ODTS (Geleast):70 mL of anhydrous toluene (Aldrich) for 30 min, followed by heating for 1 h in a convection oven to modify the Al_2O_3 surface with ODTS.[20] Figure 2(a) shows a confocal microscopy

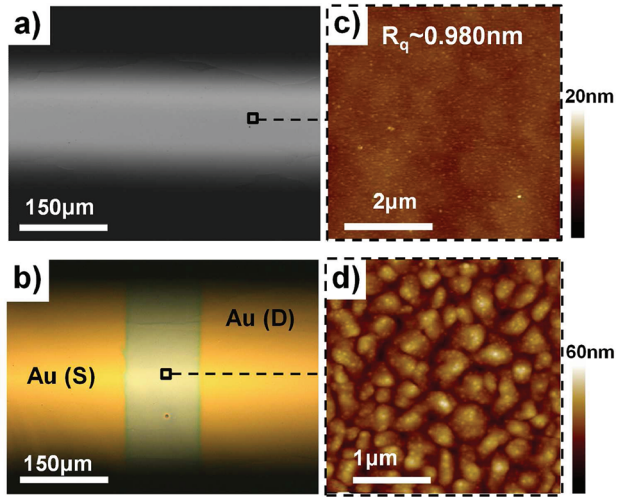


Figure 2. (a) Typical confocal microscopy image of an anodized Al wire after ODTS treatment and (b) a typical optical microscopy image of the channel area of the OFETs. Height mode AFM topographs of (c) an anodized Al wire surface and (d) a pentacene thin film on the ODTS/Al_2O_3 gate dielectric.

image (λ = 408 nm, OLS 3000, Olympus) of the very smooth surface of the ODTS modified wire. The atomic force microscopy (AFM) (Multimode SPM, Digital Instruments) topography, shown in Figure 2(b), revealed that the wire surface had an rms roughness (Rq) of 0.98 nm within the 5 × 5 μm^2 scan scale. A 50 nm-thick pentacene (Aldrich, without purification) active layer was deposited on the wire at a rate of 0.2 $Å s^{-1}$ using an organic molecular beam deposition system. Finally, the source/drain electrodes were deposited by thermal evaporation of gold (100 nm) through a shadow mask over the active layers. Because the vacuum deposition processes were carried out without rotating the substrate wire, about half of the wire was covered with the pentacene and gold electrodes.[7] Therefore, the channel width (W) could be estimated according to πR (≈ 1100 μm), and the channel length was 150 μm. Optical microscopy top-view images of the device are shown in Figure 2c. The average grain size of the pentacene active layer grown on the smooth hydrophobic ODTS-treated Al wire was approximately 0.4−0.5 μm, as can be seen in the AFM topography image in Figure 2d. The grain size was comparable to that of the pentacene films grown on an ODTS-treated SiO_2 substrate with a planar geometry.[20]

To confirm that the OFETs were fabricated properly according to the above-mentioned procedure, we investigated the cross-sections of arbitrarily selected gold source or drain electrodes. Figure 3 shows a tilted-view SEM image of a cross-section taken after focused ion beam (FIB) (FIB2200, Seiko) milling of the OFET fabricated on an Al wire substrate. The conditions for milling were 30 kV for the I-beam, and side view images were collected with a typical positive slope of 52°. We verified that each of the gold (100 nm), pentacene (50 nm), and Al_2O_3/ODTS (120 nm) layers was clearly resolved in the SEM image, as schematized in the inset of Figure 3 (upper). The lower inset image of Figure 3 presents a photograph of a

dx.doi.org/10.1021/am2011405 | ACS Appl. Mater. Interfaces 2012, 4, 6−10

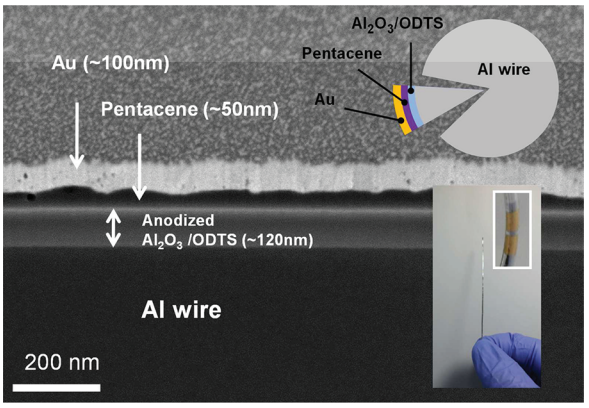


Figure 3. Tilted-view SEM image of a cross-section taken after FIB milling of the OFET fabricated on an Al wire substrate. The inset (top) shows a schematic illustration of the wire cross-section. The lower inset shows a photograph of a typical Al wire, including 12 fabricated OFETs and a magnified photographic image of a single OFET device.

typical wire that includes 12 OFETs and a magnified photographic image of a single OFET device.

Figure 4a shows typical gate voltage (V_G) versus drain current (I_D) and $I_D^{1/2}$ transfer characteristics in the saturation regime with dual V_G sweeps for the OFETs prepared on electro-poished Al wires using Al_2O_3 gate dielectrics with/without ODTS treatment. All electrical measurements were performed in ambient air using Keithley 2400 and 236 source/measure units. The field-effect mobilities (μ) were obtained from the slope of a plot of $I_D^{1/2}$ against V_G, using the equation $ID = \mu C_i(W/2L)(V_G - V_{Th})^2$, where V_{Th} and C_i are the threshold voltage and capacitance per unit area, respectively. The OFETs using ODTS/Al_2O_3 gate dielectrics exhibited high OFET performances (μ of 0.345 $cm^2\ V^{-1}\ s^{-1}$, on average) without hysteresis during the dual gate voltage sweeps in ambient air. In contrast, OFETs prepared on single Al_2O_3 gate dielectrics exhibited poor OFET performance (μ of 0.026 $cm^2\ V^{-1}\ s^{-1}$, on average) with a large hysteresis. Moreover, Al/ODTS-treated Al_2O_3/pentacene/Au metal–insulator-semiconductor-metal (MISM) diodes showed hysteresis-free operation in the capacitance–voltage (C–V) curves, as shown in Figure 4b. The averaged transistor parameters for 12 OFETs (4 OFETs in a batch, 3 batches in total) are summarized in Table 1. The average μ of 0.345 $cm^2\ V^{-1}\ s^{-1}$ was comparable with that of OFETs prepared using ODTS-modified SiO_2 gate dielectrics fabricated on planar silicon wafers.[20] The subthreshold slope (S) of the transfer curve is an important parameter and is influenced by the trap density (N_{trap}) at the interface between the pentacene and the dielectric. Using the equation below, we approximated N_{trap} for our devices

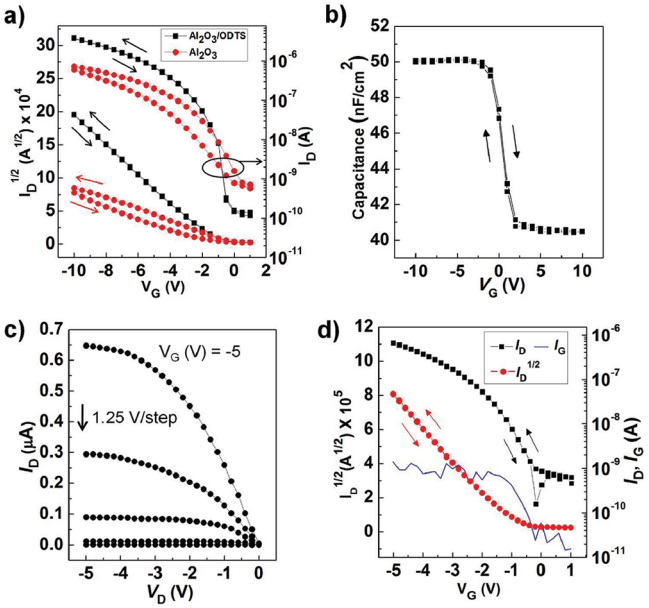


Figure 4. (a) Transfer characteristics of the OFETs prepared on electro-polished Al wires using Al_2O_3 gate dielectrics with/without ODTS treatment. (b) C–V characteristics of a MISM diode (Al/ODTS treated Al_2O_3/pentacene/Au) with dual voltage sweep. (c) Output and (d) transfer characteristics the OFETs prepared on electro-polished Al wires using ODTS/Al_2O_3 gate dielectrics operated below −5 V.

$$N_{trap} \approx \left[\frac{qSlog(e)}{kT} - 1\right]\frac{C_i}{q}$$

where q is the electronic charge, k is Boltzmann's constant, and T is the temperature.[21] The estimated N_{trap} values of the OFETs with/without ODTS treatment were 9.68×10^{11} and 7.85×10^{12} cm^{-2}, respectively. The N_{trap} of the ODTS treated devices was an order of magnitude lower than that of the untreated devices, which indicated that the ODTS treatment significantly reduced the number of interface traps between the pentacene and the Al_2O_3 gate dielectric layers.

The high capacitance and reduced N_{trap} for the ODTS-treated Al_2O_3 gate dielectrics facilitated the low-voltage high-performance operation of the OFETs prepared on electro-polished Al wires. Figure 4c shows typical drain voltage (V_D) versus I_D output characteristics of the OFETs using ODTS/Al_2O_3 gate dielectrics, showing good linear/saturation behavior within the operating voltage range of −5 V, without a leakage current at zero V_D. Although the single Al_2O_3 gate dielectrics yielded a higher capacitance than the ODTS/Al_2O_3 gate dielectrics, the OFETs prepared using single Al_2O_3 gate dielectrics failed to operate at −5 V due to the high N_{trap}. The transfer characteristics and gate leakage current for the V_G sweeps up to −5 V, for OFETs with ODTS/Al_2O_3 gate dielectrics, are shown in Figure 4d. The OFETs with ODTS/Al_2O_3 gate dielectrics also exhibited high-performance hysteresis-free operation below −5 V, and the gate leakage current was below 1.5 nA.

Table 1. Transistor Parameters for the Pentacene-Based OFETs Prepared on Electro-Polished Al Wires Using Al_2O_3 Gate Dielectrics with/without ODTS Treatment

dielectric	C_i (nF cm^{-2})	μ ($cm^2\ V^{-1}\ s^{-1}$)	V_{Th} (V)	on/off ratio	S (mV $decade^{-1}$)	N_{trap} (cm^{-2})
Al_2O_3	53.2	0.026 (± 0.02)	2.04 (± 0.35)	~1×10^3	1.438 (± 0.28)	7.85×10^{12}
Al_2O_3/ODTS	50.1	0.345 (± 0.04)	−0.98 (± 0.12)	~1×10^4	0.242 (± 0.04)	9.68×10^{11}

dx.doi.org/10.1021/am2011405 | ACS Appl. Mater. Interfaces 2012, 4, 6–10

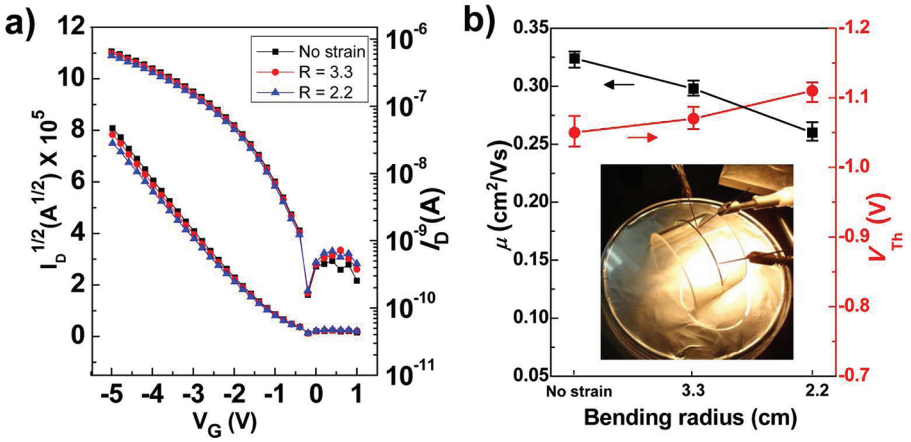


Figure 5. (a) V_G versus I_D, and $I_D^{1/2}$ transfer characteristics of the OFETs prepared on Al wires as a function of the R. (b) Variations in μ and V_{Th} of the devices as a function of the R. The inset digital camera image of b illustrates a cylindrical wire involving 8 OFET devices in a bent state during electrical measurements.

A question may arise: Is the performance of our OFETs on Al wires comparable to that of the devices prepared on planar-type substrates having the same device configuration? To answer this question, we fabricated pentacene-based OFETs on an Al foil gate laminated on a polymer substrate. The device was fabricated as previously reported and detailed procedure is summarized as schematics in the Supporting Information, Figure S1.[17] As shown in the Supporting Information, Figure S2, the devices on an Al wire (i.e., wire devices) exhibited better performance than the devices on an Al foil (i.e., foil devices). We speculate that the higher performance of the wire devices results from the lower gate dielectric surface roughness of the wire devices (R_q = 0.98 nm) when compared to the foil devices (R_q = 2.12 nm) (see AFM images in Figure 2c and the Supporting Information, Figure S1).

To investigate the mechanical stress-durability of the OFETs prepared on Al wires, bending experiments were performed on the devices. Two types of half-round glass tubes with different diameters (see the Supporting Information, Figure S3) were used to apply a constant tensile strain during an electrical measurement, as illustrated in the inset of Figure 5b. Figure 5a shows the transfer characteristics as a function of the bending radius (R), and Figure 5b shows the relationship between R and μ and between R and V_{Th} for the OFETs. As presented in Figure 5, the devices maintained good transistor performances even at a tensile strain of $R \approx 2.2$; the μ values retained over 80% of their initial value, and the V_{Th} values decreased from their initial level by only 5%. To the best of our knowledge, $R \approx 2.2$ is much lower value than the minimum value of R reported thus far ($R \approx 8.0$) for the OFETs prepared on cylindrical fiber-shaped substrates.[8]

In summary, we prepared high-performance low-voltage operating pentacene-based OFETs with high bending-stability on an Al wire substrate. The Al wire substrate surface was smoothed by 10 min of an electro-polishing process. An anodized Al_2O_3 gate dielectric was developed around the wire, and ODTS was applied to modify the gate dielectric surface using solution processes. The ODTS/Al_2O_3 gate dielectrics showed a high capacitance of 50.1 nF cm^{-2} and reduced N_{trap} at the interface between the pentacene layer and the dielectric. The OFETs prepared using ODTS/Al_2O_3 gate dielectrics exhibited high-performance, hysteresis-free, and bending stress-durable operation in ambient air within a low operating voltage range of −5 V.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Detailed description of the fabrication setup of the pentacene-based OFETs on an Al foil gate laminated on a polymer substrate, including the AFM image of the gate dielectric surface and the digital camera image of the overall device. Transfer characteristics of the OFETs on an Al wire substrate and the OFETs on an Al foil substrate, and their transistor parameters. Detailed conditions of bending experiment of the OFETs on an Al wire substrate. This material is available free of charge via the Internet at http://pubs.acs.org/.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: cep@postech.ac.kr; jongkim@samsung.com.

Author Contributions

[§]These authors contributed equally to this work.

■ ACKNOWLEDGMENTS

This work was supported by a grant from the Korea Science and Engineering Foundation (KOSEF), funded by the Korea government (MEST) (20110000330).

■ REFERENCES

(1) Forrest, S. R. *Nature* **2004**, *428*, 911.
(2) Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. *Nat. Mater.* **2010**, *9*, 1015.
(3) Street, R. A.; Wong, W. S.; Ready, S. E.; Chabinyc, M. L.; Arias, A. C.; Limb, S.; Salleo, A.; Lujan, R. *Mater. Today* **2006**, *9*, 32.
(4) Zschieschang, U.; Yamamoto, T.; Takimiya, K.; Kuwabara, H.; Ikeda, M.; Sekitani, T.; Someya, T.; Klauk, H. *Adv. Mater.* **2011**, *23*, 654.
(5) Hamedi, M.; Forchheimer, R.; Inganäs, O. *Nat. Mater.* **2007**, *6*, 357.
(6) Hamedi, M.; Herlogsson, L.; Crispin, X.; Marcilla, R.; Berggren, M.; Inganäs, O. *Adv. Mater.* **2009**, *21*, 573.
(7) Maccioni, M.; Orgiu, E.; Cosseddu, P.; Locci, S.; Bonfiglio, A. *Appl. Phys. Lett.* **2006**, *89*, 143515.
(8) Lee, J. B.; Subramanian, V. *IEEE Trans. Electron Devices* **2005**, *52*, 269.
(9) Granstrom, J.; Katz, H. *J. Mater. Res.* **2004**, *19*, 3540.

(10) Lee, J. B.; Subramanian, V. *IEEE Int. Electron Devices Meet.* **2003**, 8.3.1−8.3.4.
(11) Liu, J.; Namboothiry, M. A. G.; Carroll, D. L. *Appl. Phys. Lett.* **2007**, *90*, 063501.
(12) Veres, J.; Ogier, S.; Lloyd, G. *Chem. Mater.* **2004**, *16*, 4543.
(13) Lee, J.; Kaake, L. G.; Cho, J. H.; Zhu, X.-Y.; Lodge, T. P.; Frisbie, C. D. *J. Phys. Chem. C* **2009**, *113*, 8972.
(14) Kalb, W. L.; Mathis, T.; Haas, S.; Stassen, A. F.; Batlogg, B. *Appl. Phys. Lett.* **2007**, *90*, 092104.
(15) Jo, P. S.; Sung, J.; Park, C.; Kim, E.; Ryu, D. Y.; Pyo, S.; Kim, H.-C.; Hong, J. M. *Adv. Func. Mater.* **2008**, *18*, 1202.
(16) Zhao, Y.-P.; Wang, G.-C.; Lu, T.-M. *Phys. Rev. B* **1999**, *60*, 9157.
(17) Yang, C.; Shin, K.; Yang, S. Y.; Jeon, H.; Choi, D.; Chung, D. S.; Park, C. E. *Appl. Phys. Lett.* **2006**, *89*, 153508.
(18) Jang, J.; Nam, S.; Yun, W. M.; Yang, C.; Hwang, J.; An, T. K.; Chung, D. S.; Park, C. E. *J. Mater. Chem.* **2011**, *21*, 12542.
(19) Majewski, L. A.; Schroeder, R.; Grell, M. *Adv. Mater.* **2005**, *17*, 192.
(20) Lee, H. S.; Kim, D. H.; Cho, J. H.; Hwang, M.; Jang, Y. S.; Cho, K. *J. Am. Chem. Soc.* **2008**, *130*, 10556.
(21) McDowell, M.; Hill, I. G.; McDermott, J. E.; Bernasek, S. L.; Schwartz, J. *Appl. Phys. Lett.* **2006**, *88*, 073505.